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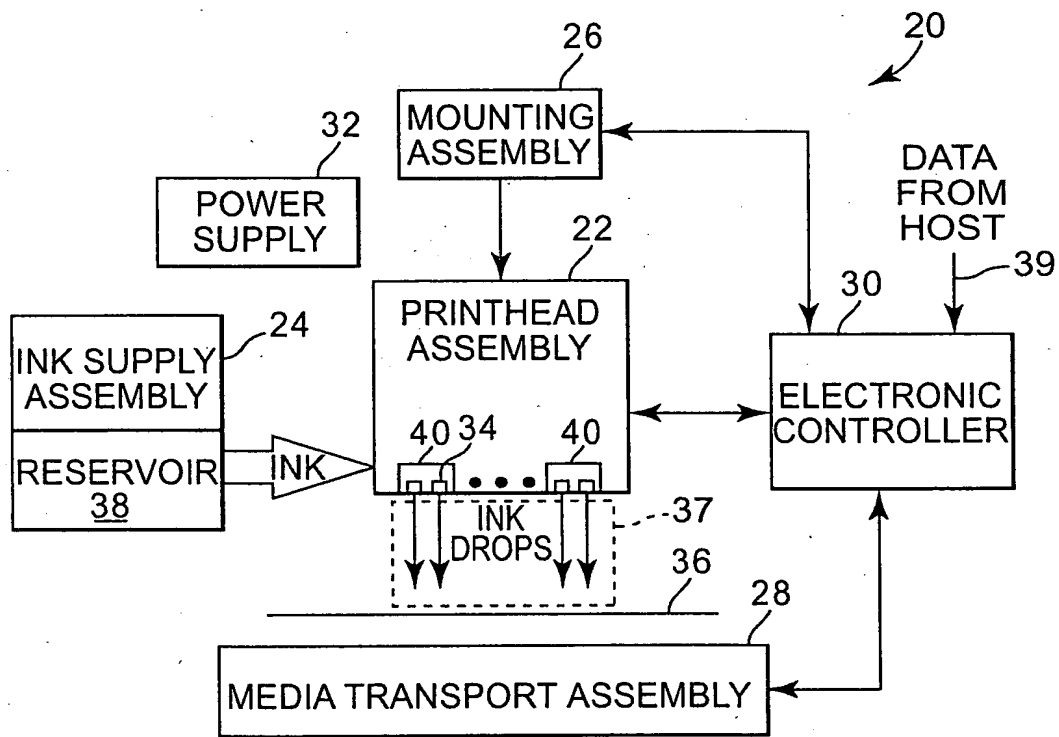


Fig. 1

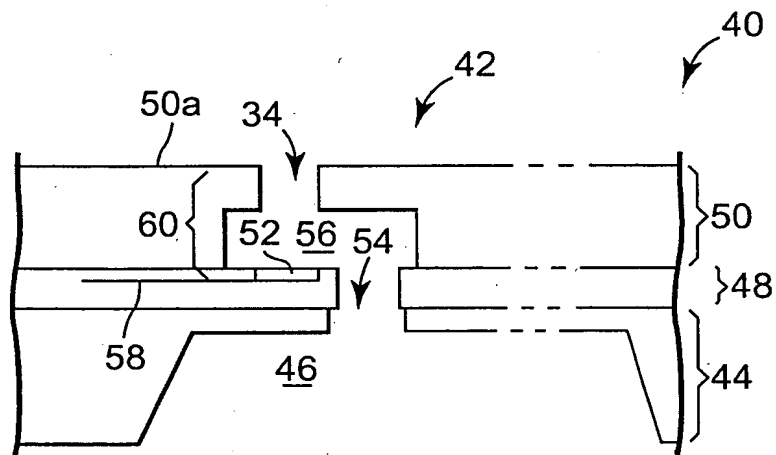


Fig. 2

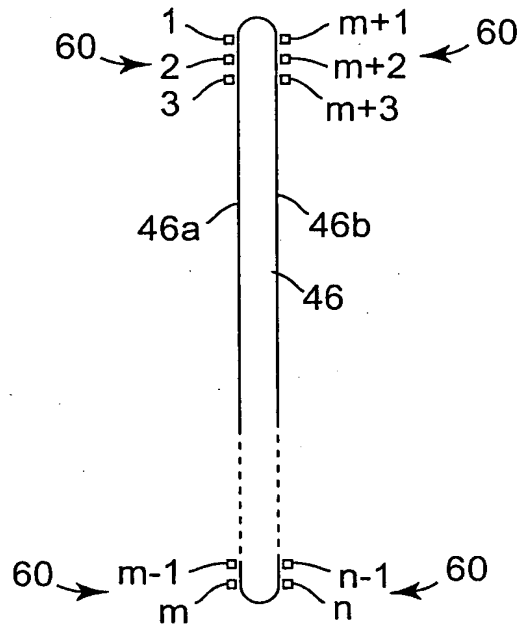


Fig. 3

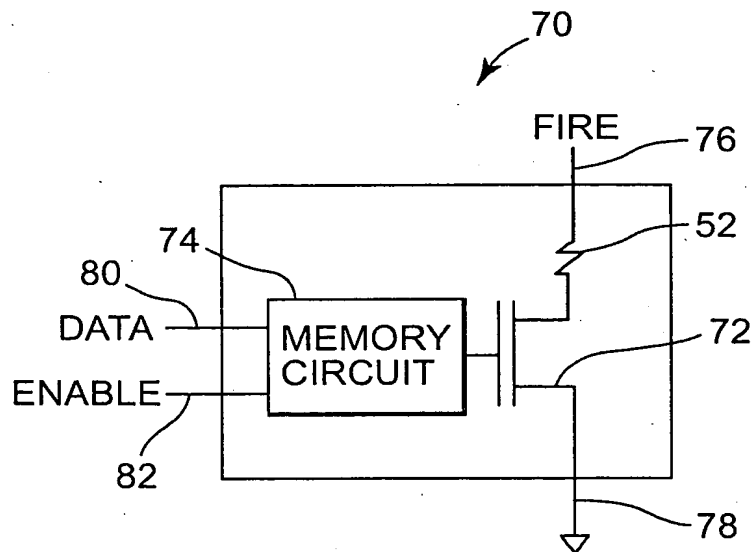


Fig. 4

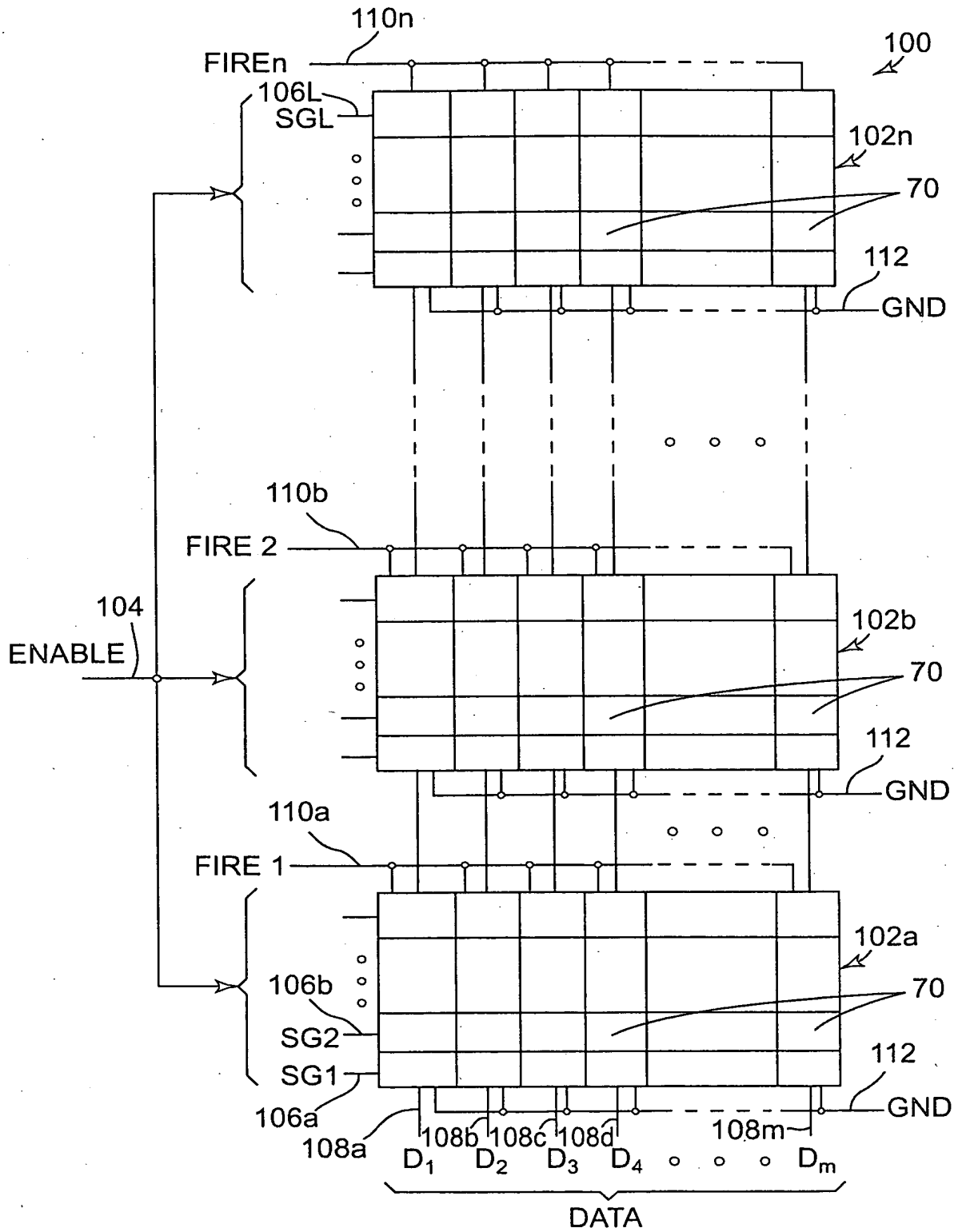


Fig. 5

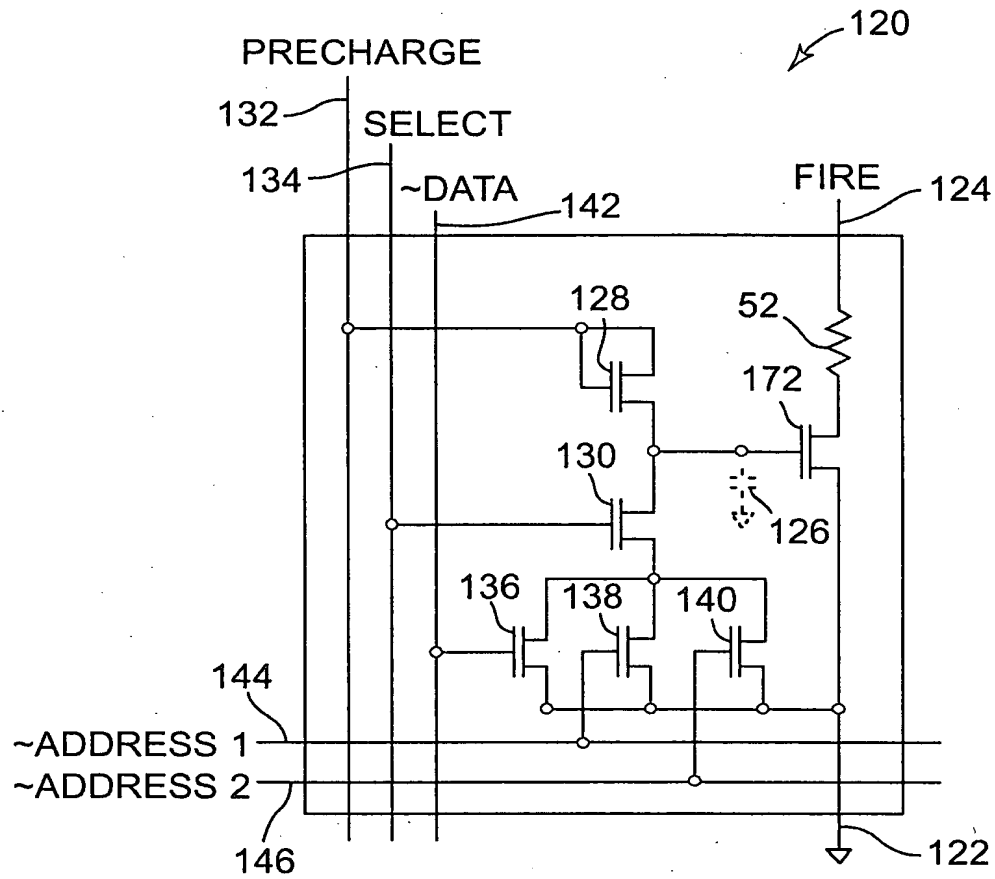


Fig. 6

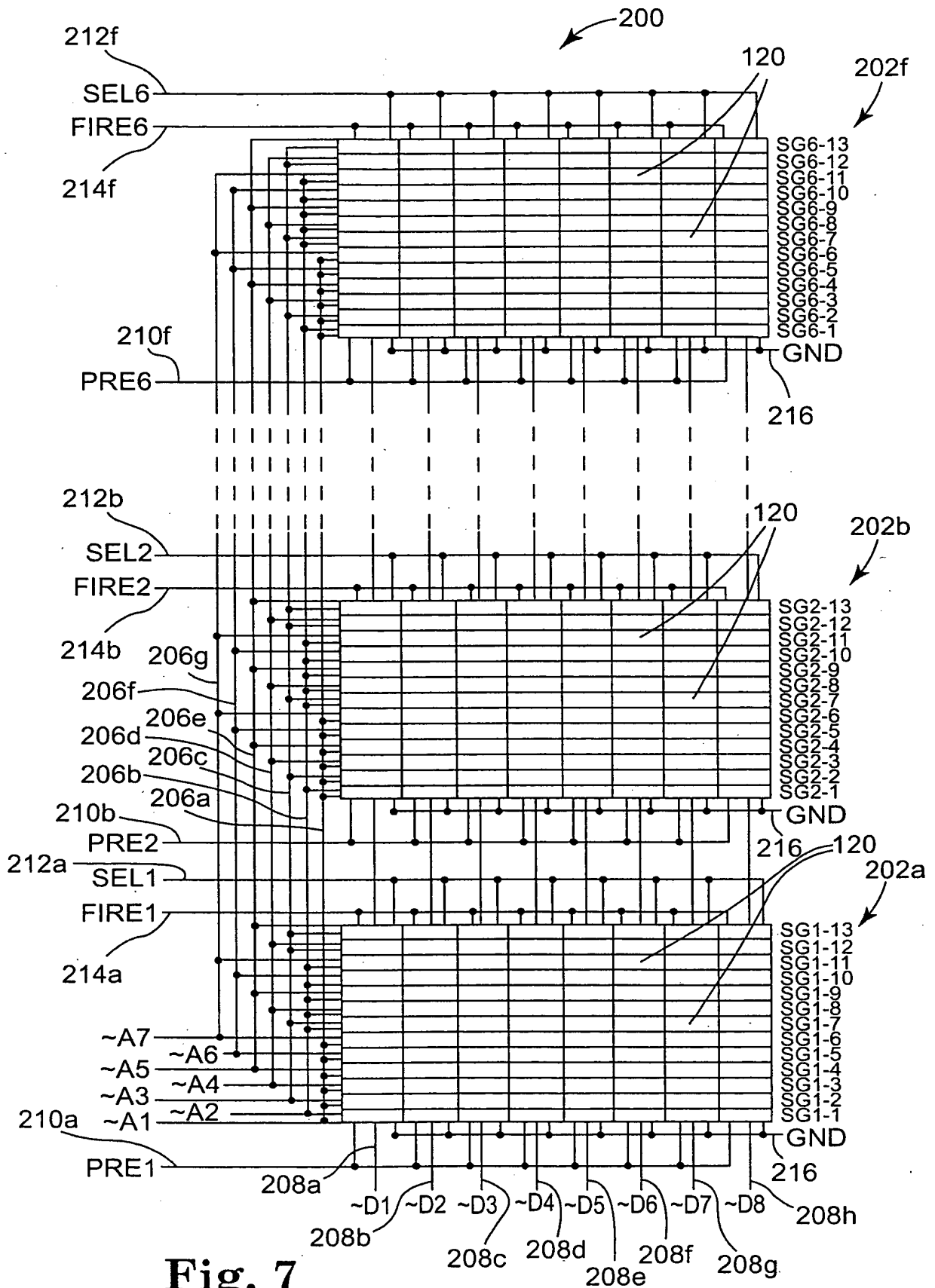


Fig. 7

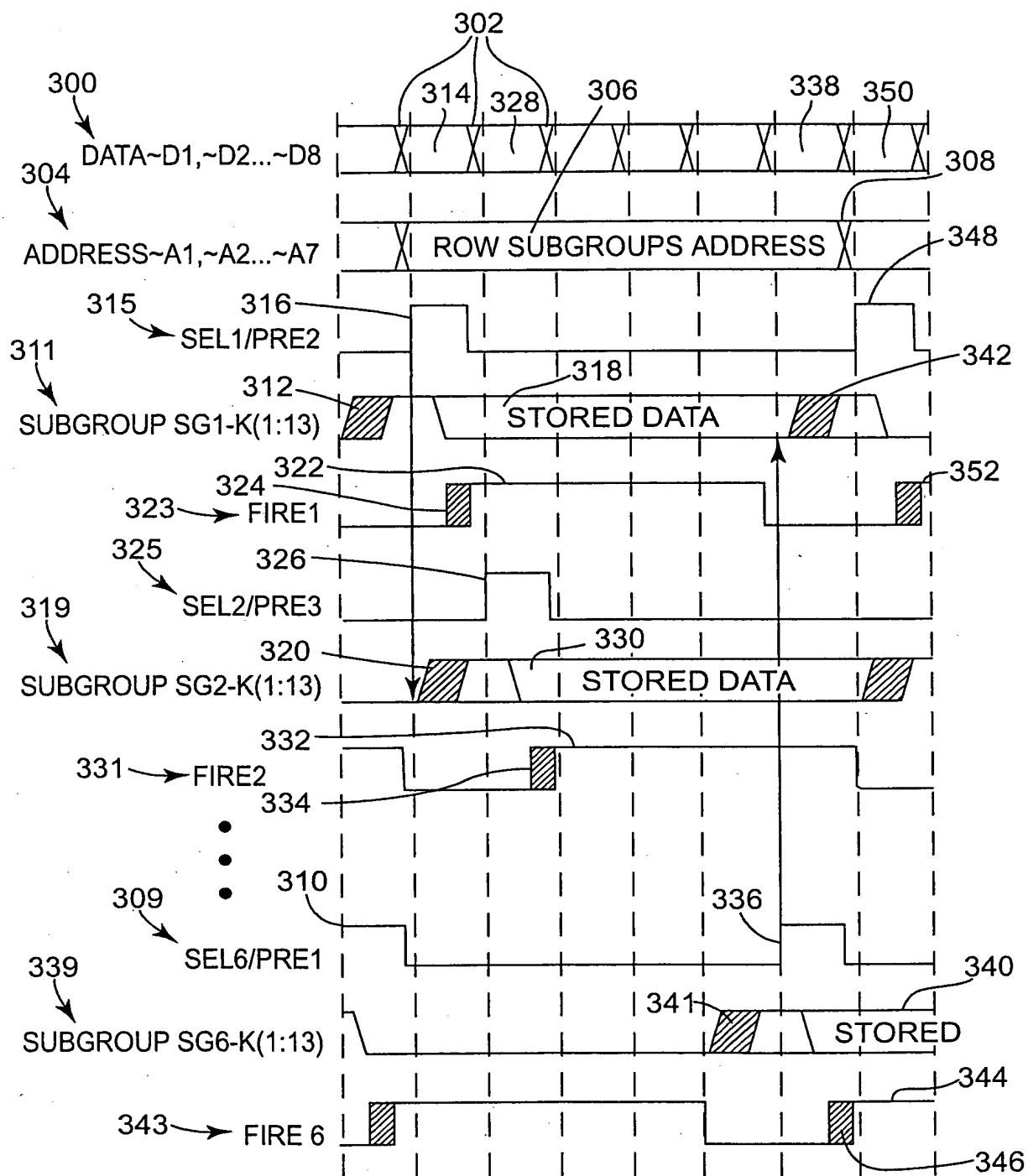


Fig. 8

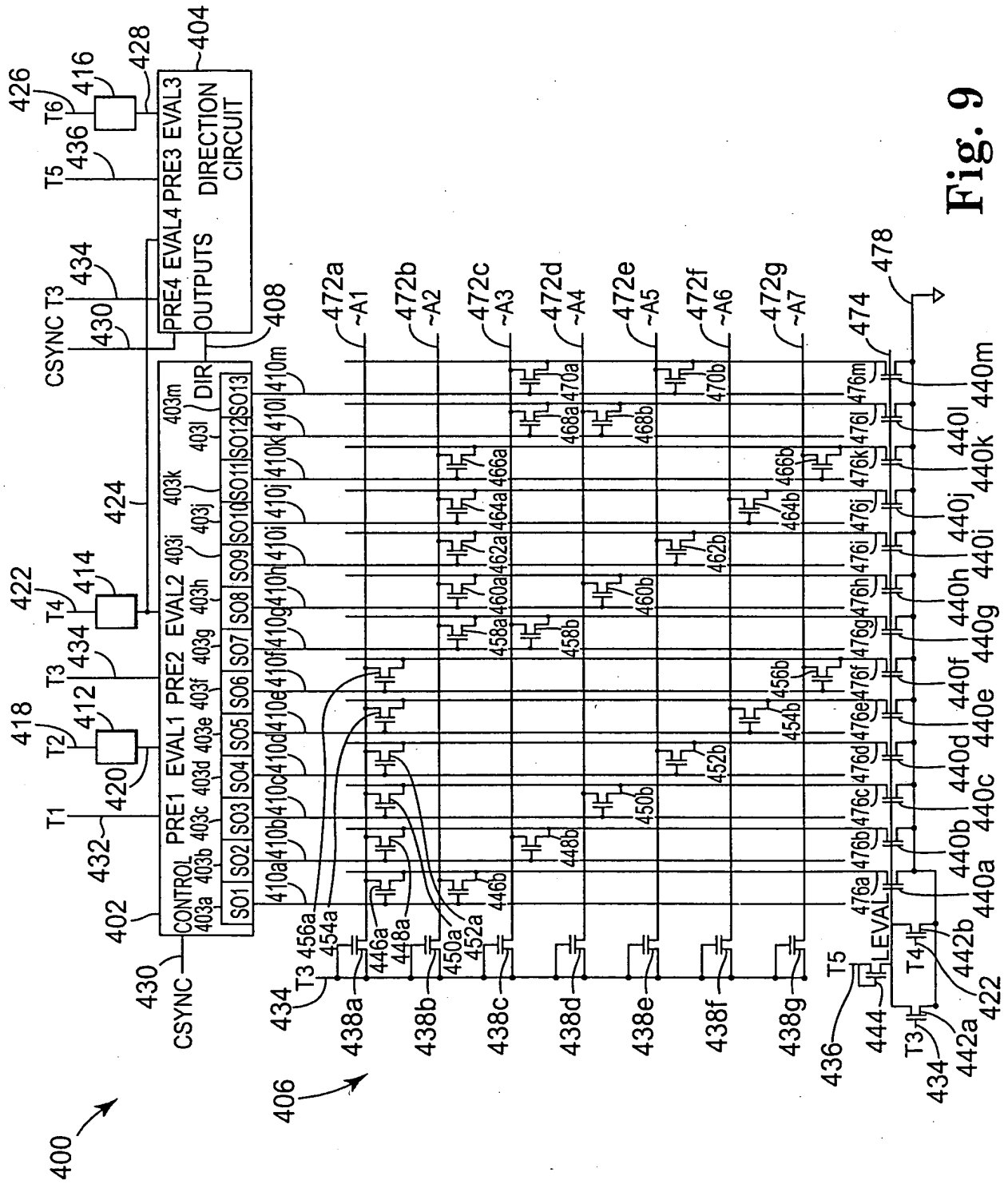


Fig. 9

The figure shows two circuit diagrams, 550 and 552, which are differential signal processing stages. Both are contained within a larger block labeled 404.

Diagram 550 (Left): This circuit has two inputs: EVAL3 and PRE3. EVAL3 is connected to a node 428, which is the gate of a PMOS transistor 554. The source of 554 is connected to a node 436, which is also the gate of an NMOS transistor 556. The source of 556 is connected to a node 430, which is the gate of another NMOS transistor 558. The source of 558 is connected to ground (568). The drain of 554 is connected to a node 408a, which is labeled DIRF. The drain of 556 is connected to a node 566.

Diagram 552 (Right): This circuit has two inputs: EVAL4 and PRE4. EVAL4 is connected to a node 424, which is the gate of a PMOS transistor 560. The source of 560 is connected to a node 434, which is also the gate of an NMOS transistor 562. The source of 562 is connected to a node 430, which is the gate of another NMOS transistor 564. The source of 564 is connected to ground (572). The drain of 560 is connected to a node 408b, which is labeled DIRR. The drain of 562 is connected to a node 570.

Fig. 10B

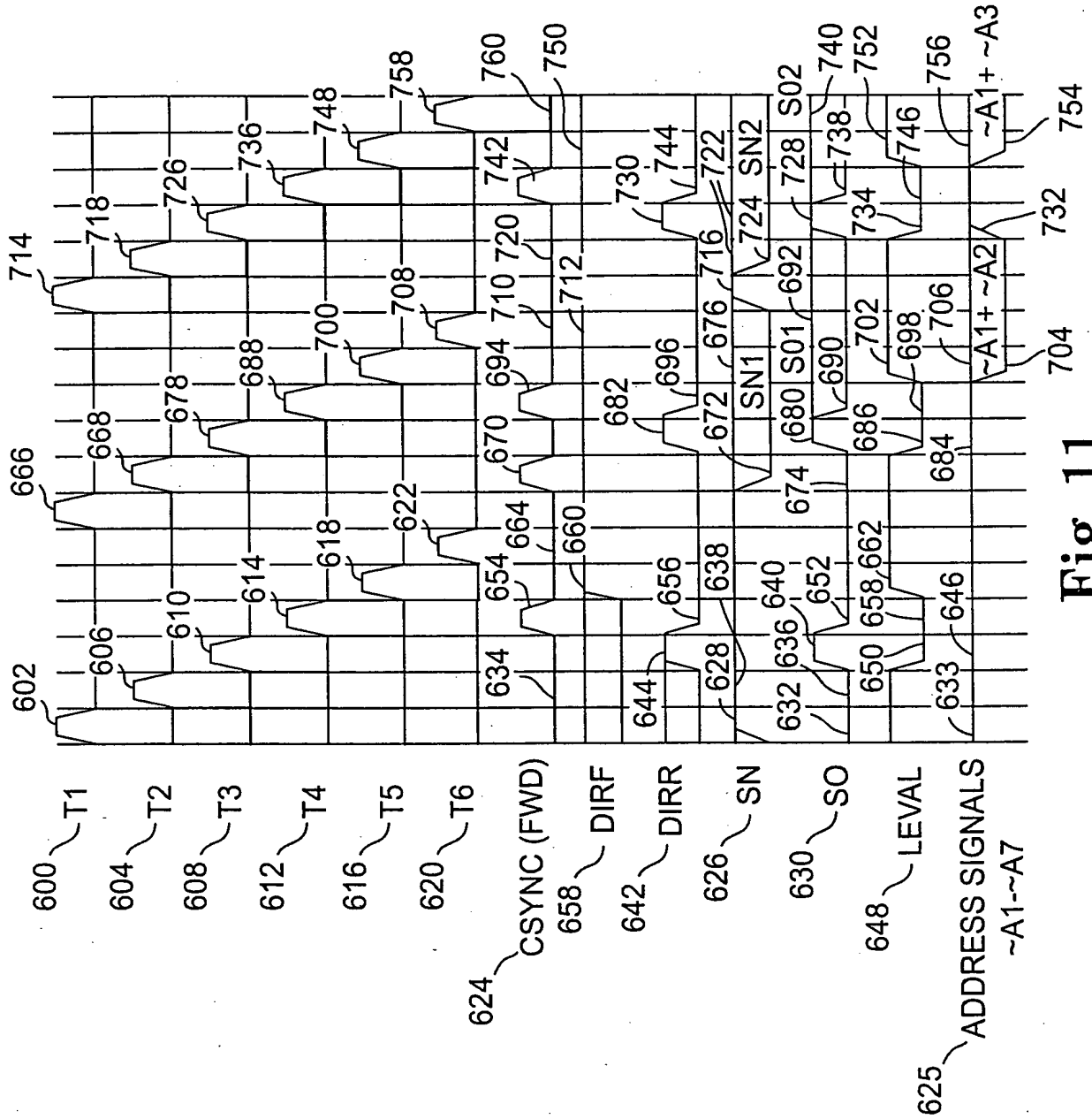


Fig. 11

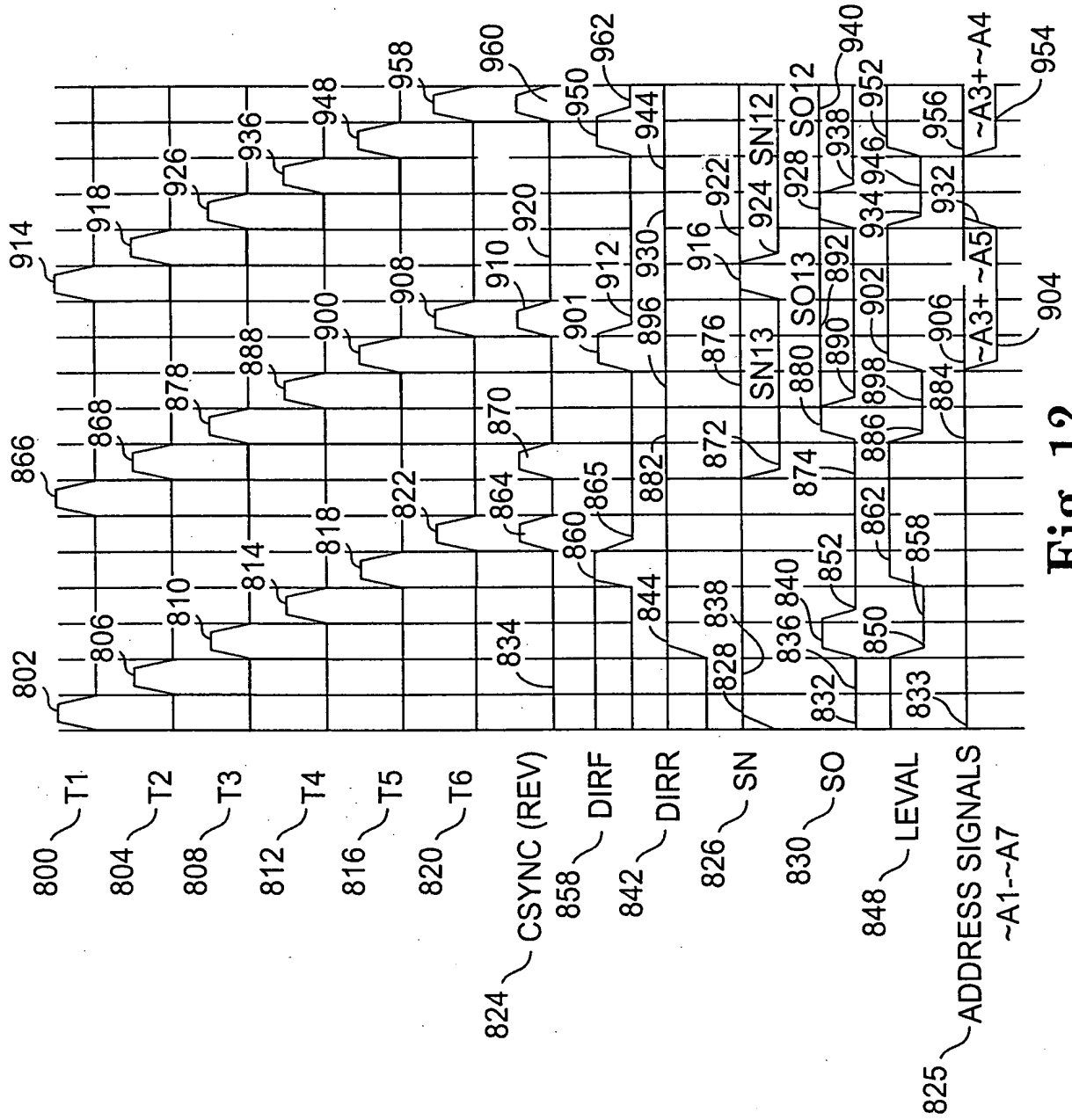


Fig. 12

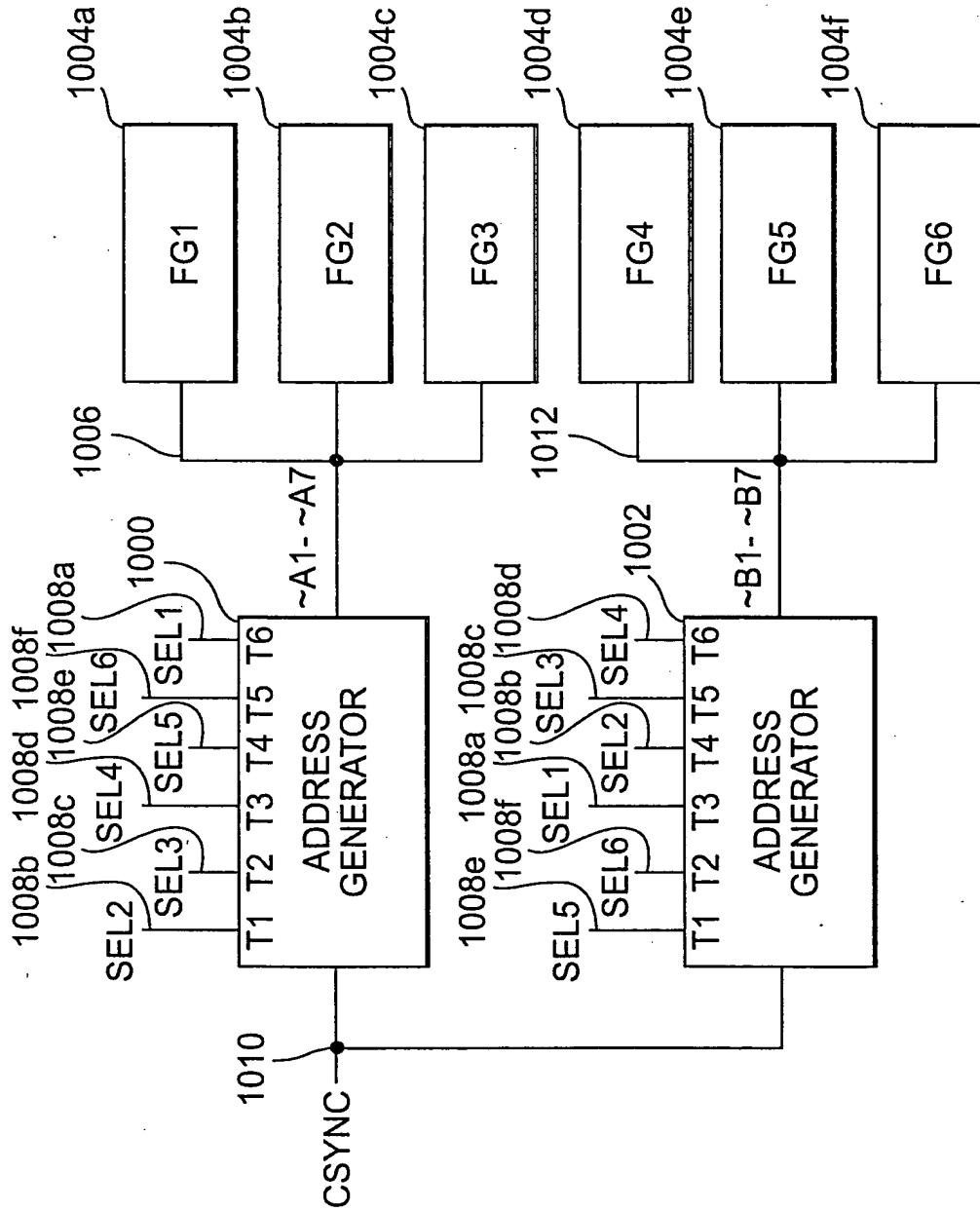


Fig. 13

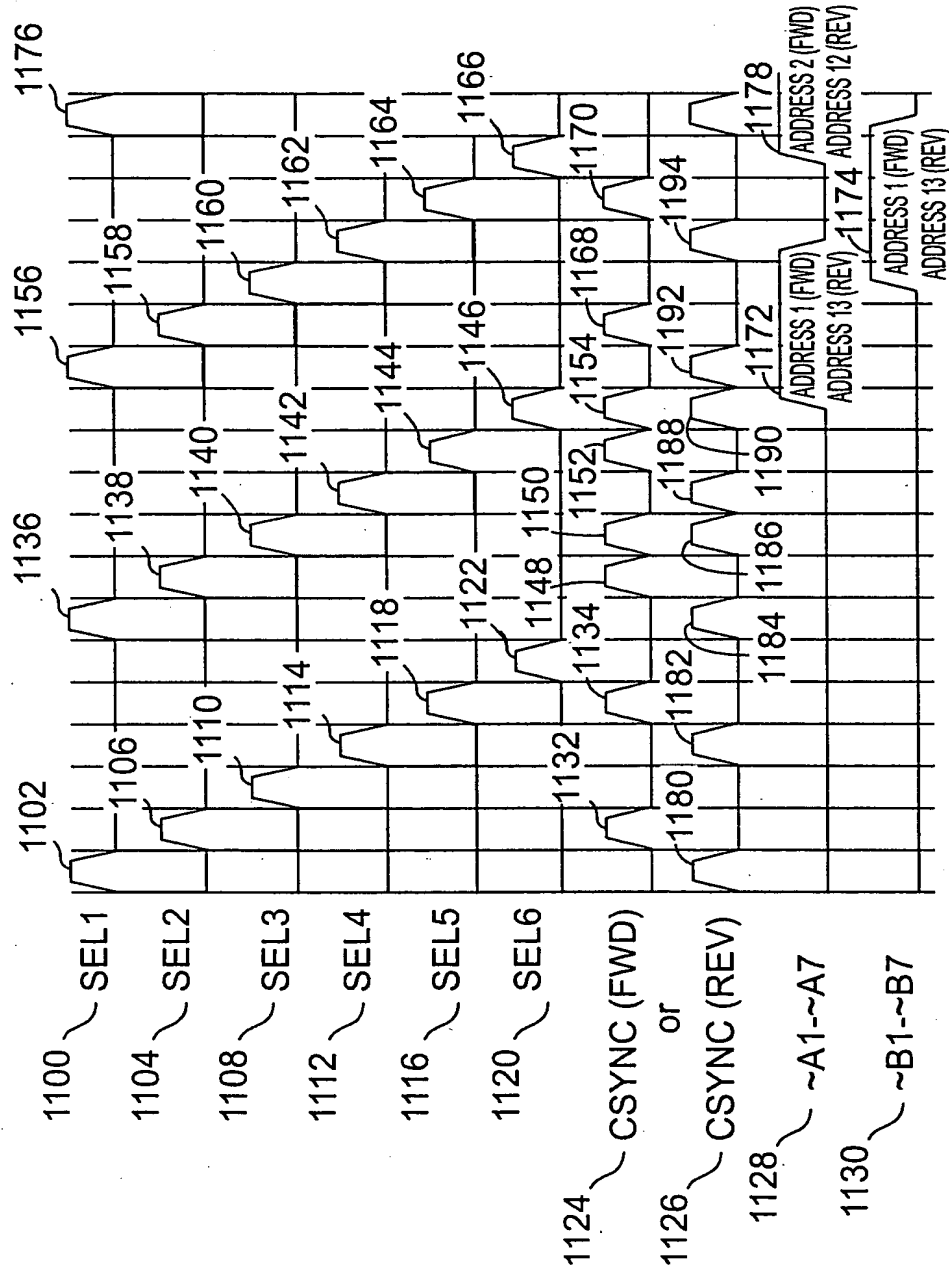


Fig. 14

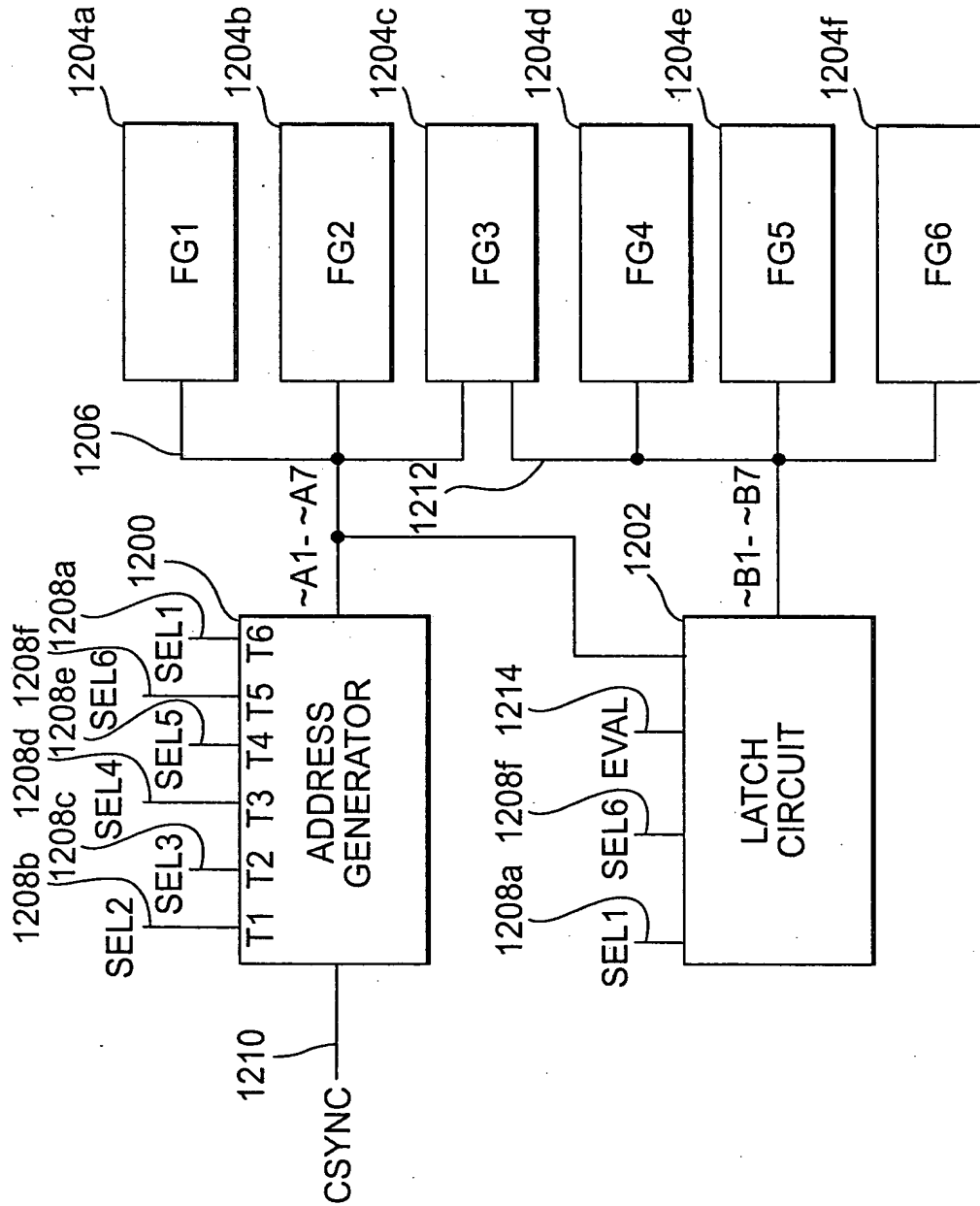


Fig. 15

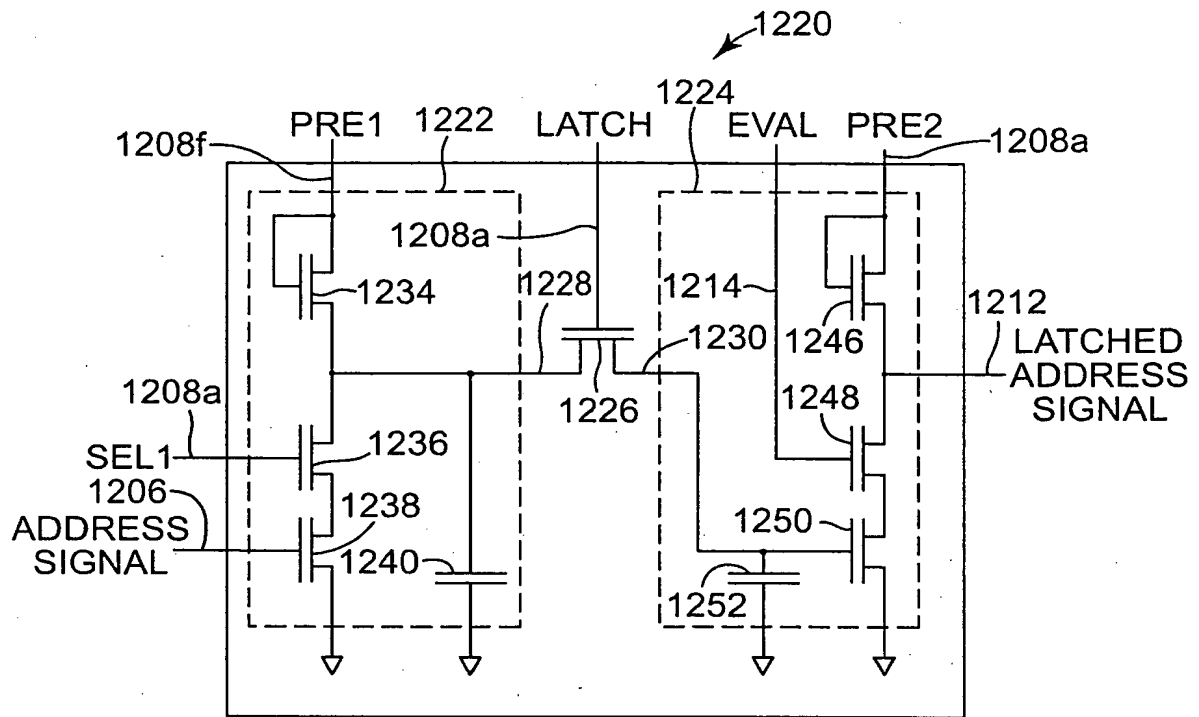


Fig. 16

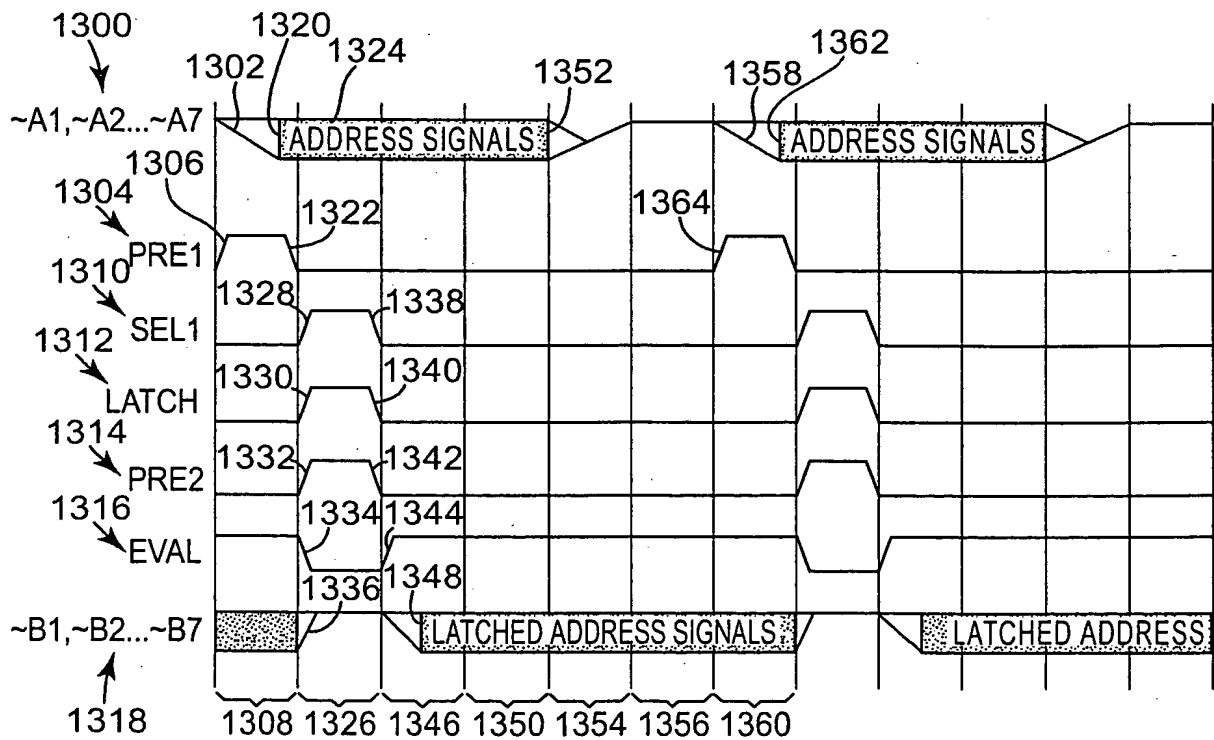


Fig. 17

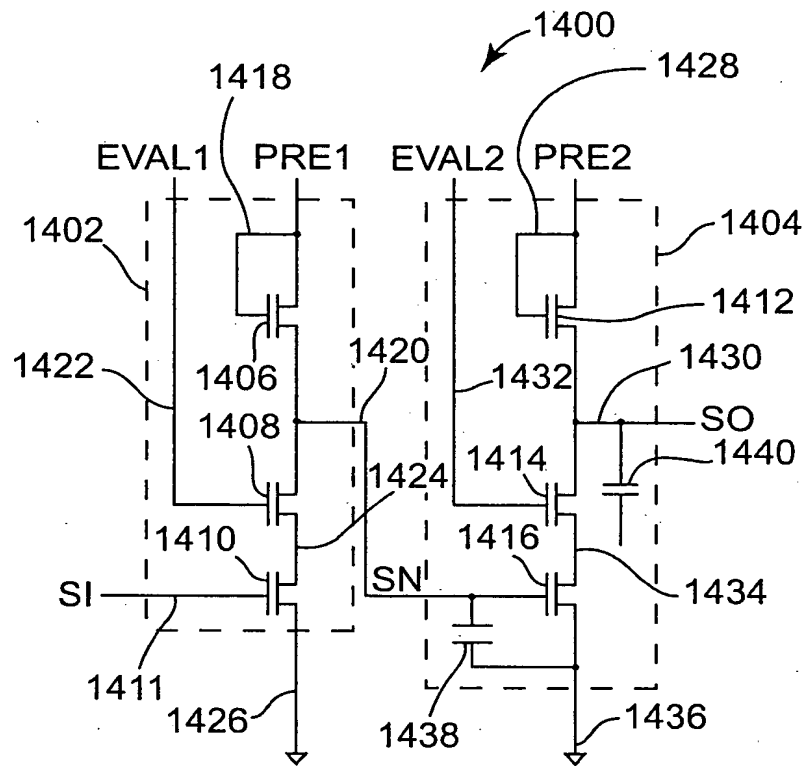


Fig. 18

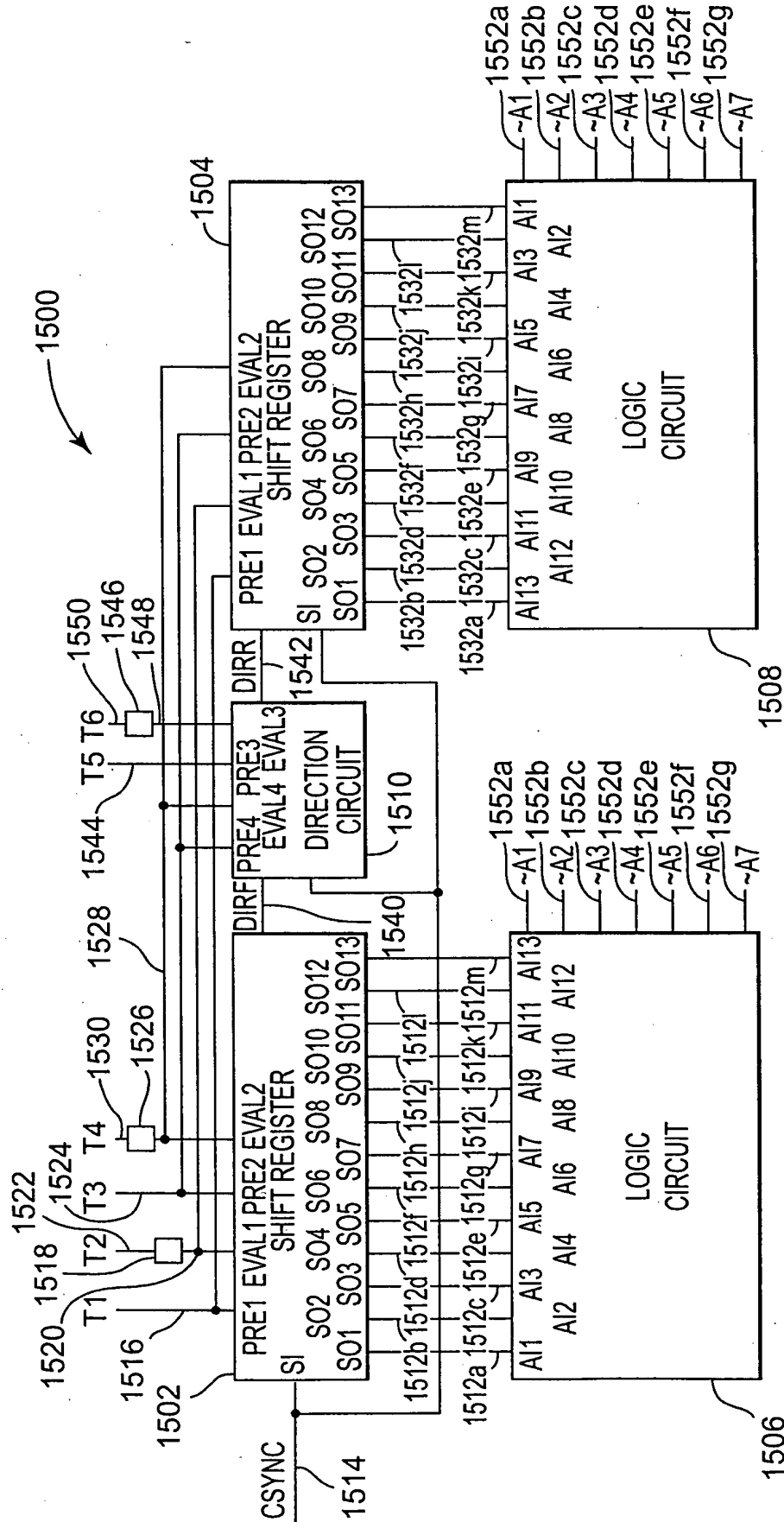


Fig. 19

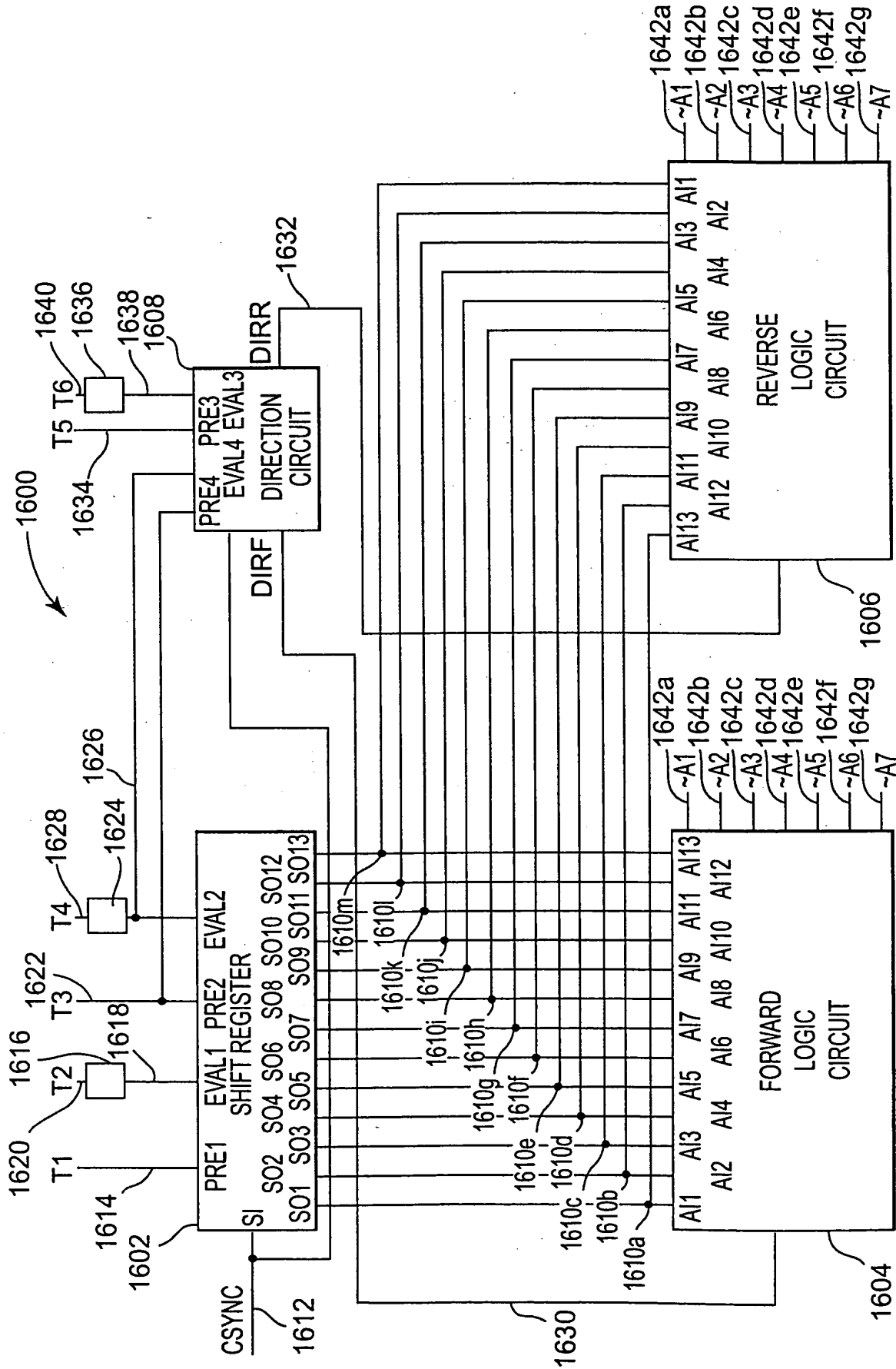


Fig. 20

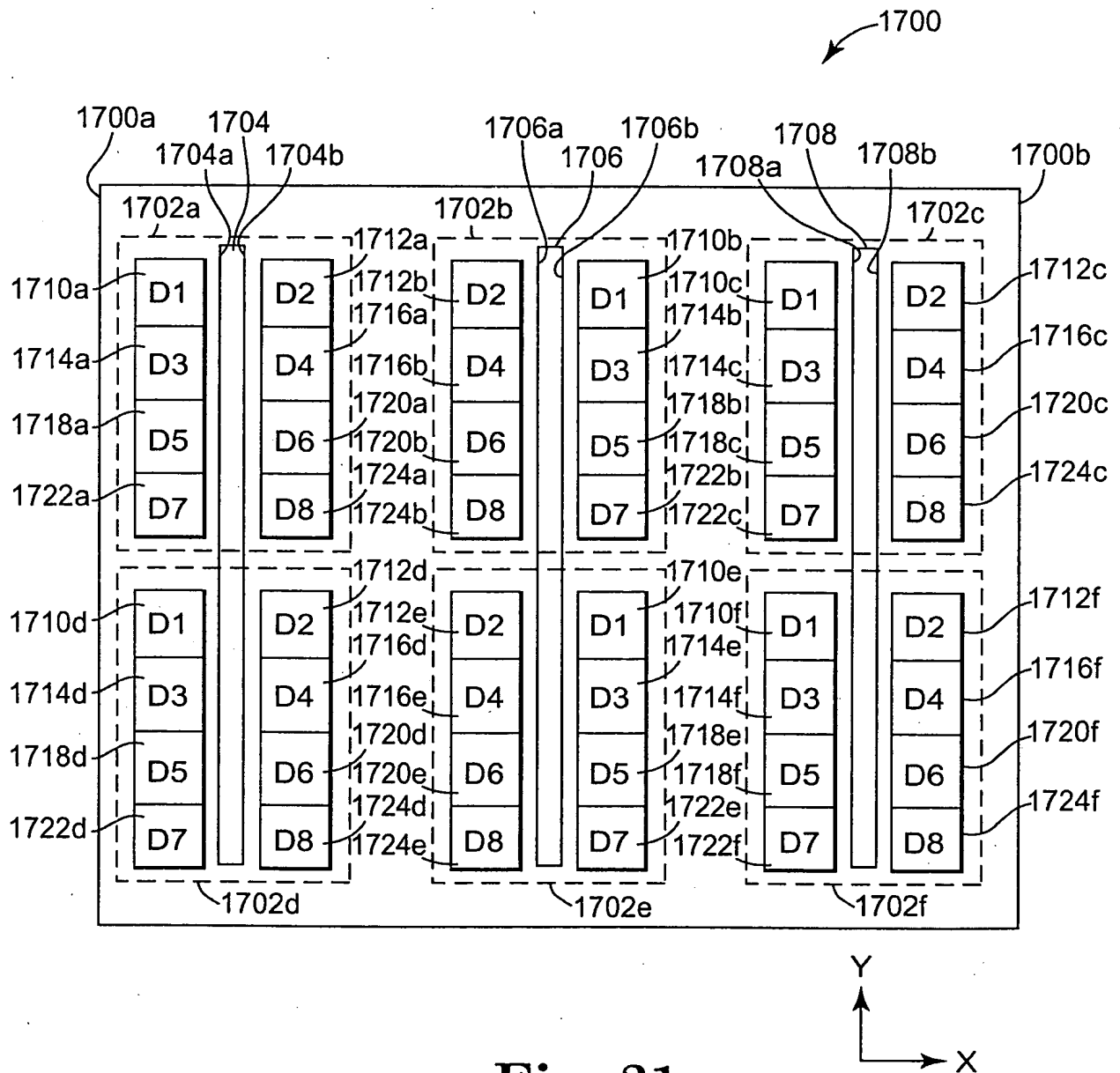


Fig. 21

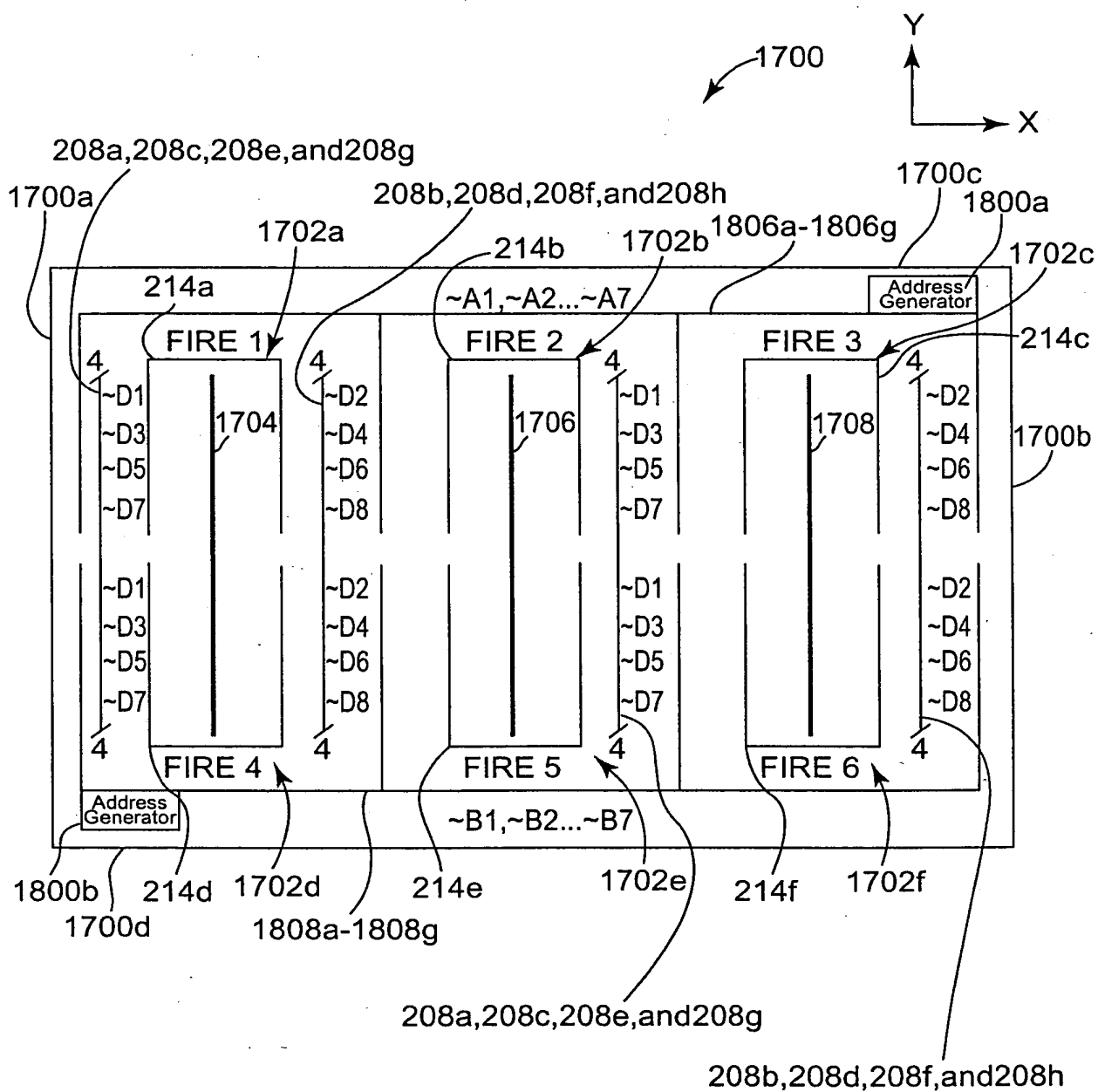


Fig. 22

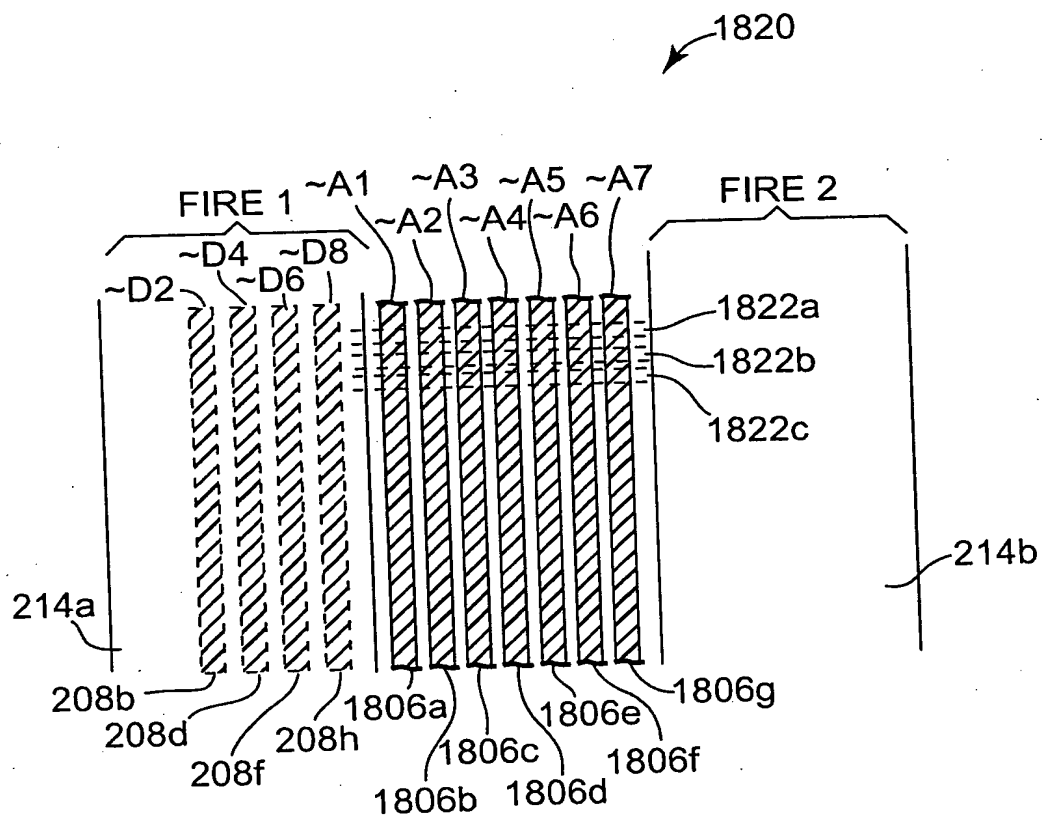


Fig. 23

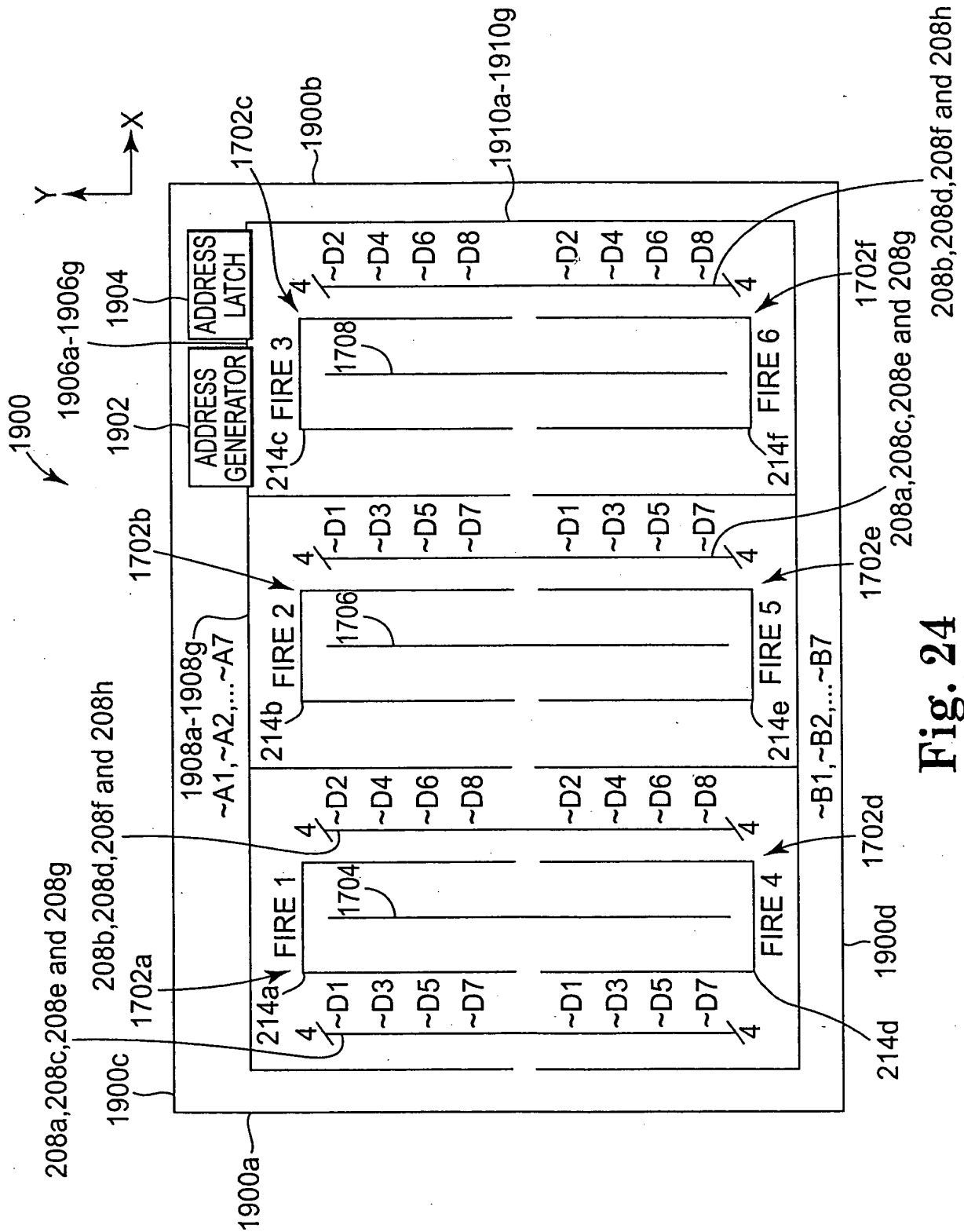


Fig. 24

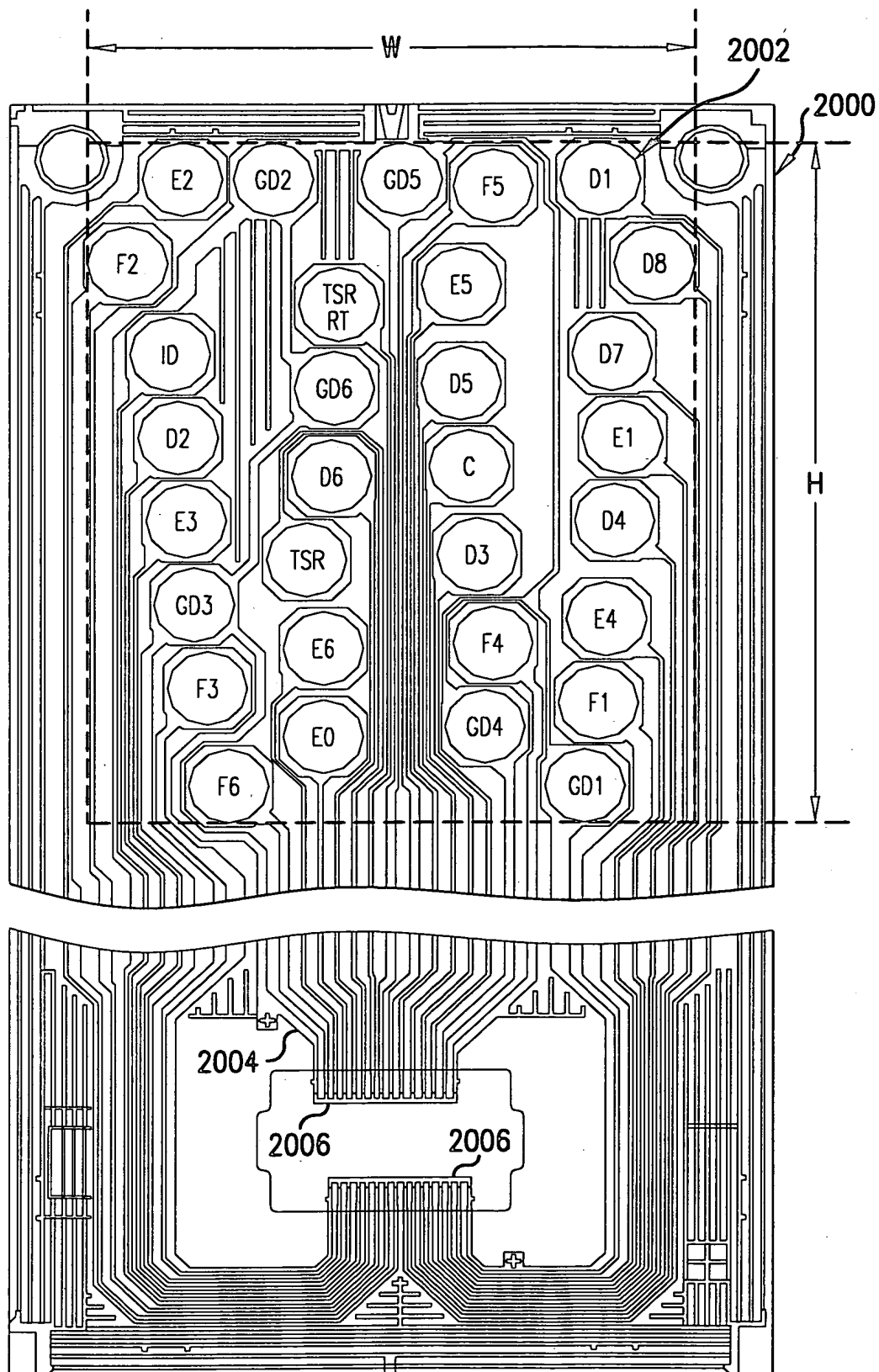


FIG. 25A

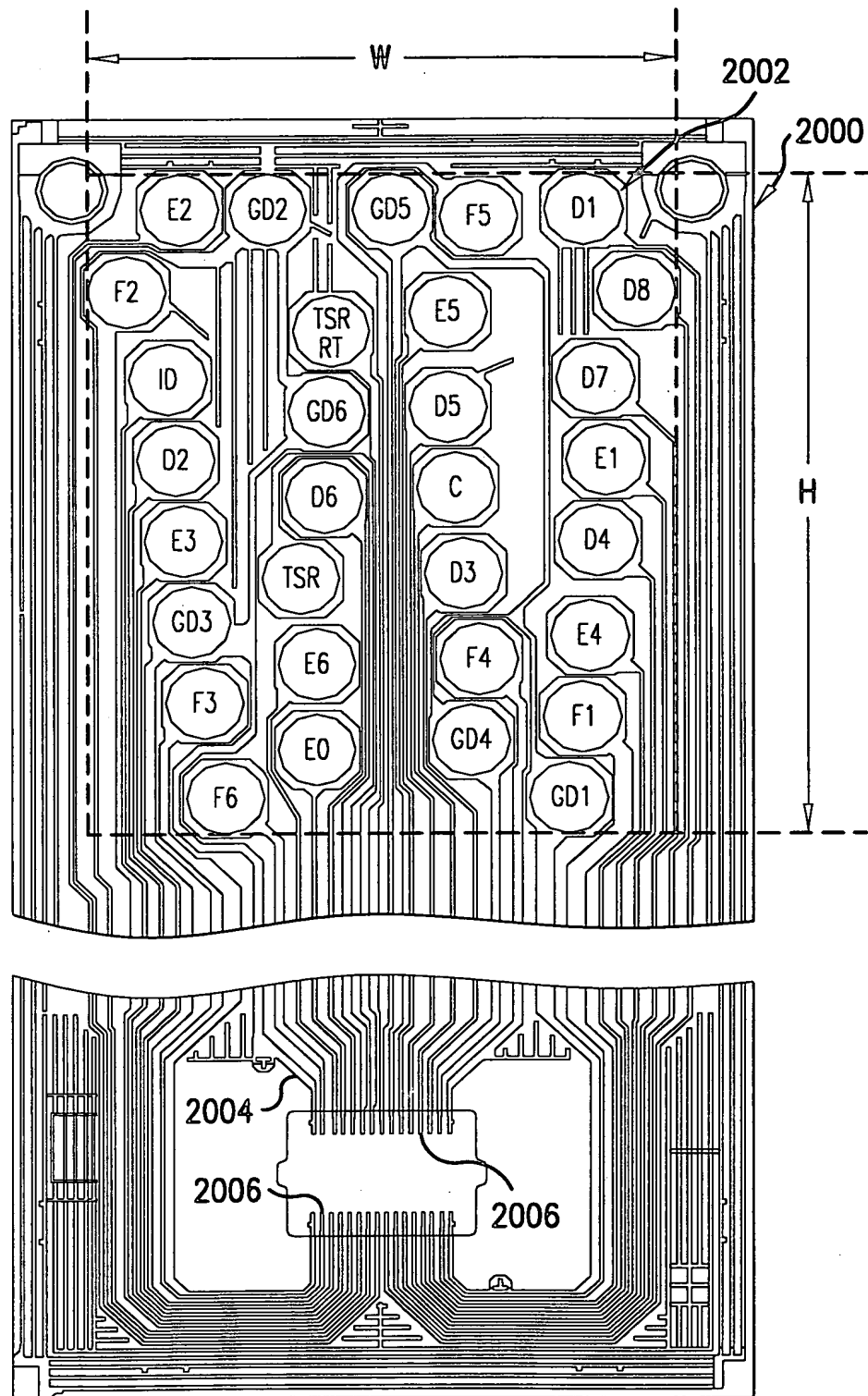


FIG. 25B